IN THE CLAIMS:

This listing of claims replaces all prior versions.

1. (Currently Amended) A bi-stable latch circuit having a pair of cross-coupled branches, each branch including a ~~complementary~~ driver and a load, the branch connected between a drain line and a source line, and each branch ~~also including~~providing a non-volatile memory cell having a program transistor and a read transistor, ~~comprising:~~wherein:

at least one of the ~~drivers~~driver and ~~loads~~load of a branch includes ~~a~~the corresponding read transistor;

said driver and load of ~~said~~each branch are connected in series ~~at~~and provide a respective output node;

said read transistor and said program transistor of each branch have a common floating gate (13,14) and separate control gates;

~~said~~each control gate of ~~said~~each program transistor is ~~connected~~connectable to a program voltage;

~~the~~a drain of ~~said~~each program transistor is connected to a respective input node; ~~and~~

said control gate of said read transistor in ~~said~~each branch is connected to the output node of the other branch~~.~~; and

wherein said drain and source line are connectable across a common supply voltage in static mode and at least one of said drain and source lines is disconnectable from said common supply voltage in a program mode.

2. (Currently Amended) The bi-stable latch circuit according to claim 1, wherein at least one of said read transistor ~~or~~and said program transistor is a semiconductor device using hot electron injection for changing a threshold voltage thereof.

3. (Cancelled)

4. (Currently Amended) The bi-stable latch circuit according to claim 1, wherein the ~~inputs~~input nodes are held at logic low level in said static mode but the voltage at one of said ~~inputs~~input nodes is raised to a voltage level, high enough to generate hot electrons or hot holes

at the drain of ~~a~~the respective program transistor in a program mode.

5. (Currently Amended) The latch circuit according to claim ~~4~~,1, wherein said program voltage is connected to said common supply voltage in said static mode but said program voltage level is raised to a voltage high enough to attract electrons or holes into said floating gate in said program mode.

6. (Cancelled)

7. (Currently Amended) A method for programming a bi-stable latch circuit, the bi-stable latch circuit having a pair of cross-coupled branches, each branch including a ~~complementary~~ driver and a load, the branches connected between a drain line and a source line, and each branch ~~also including~~providing a non-volatile memory cell having a program transistor and a read transistor, ~~comprisingaccording to claim 1 comprising:~~and wherein:

at least one of the driver and load of a branch includes the corresponding read transistor;

said driver and load of each branch are connected in series and provide a respective output node;

said read transistor and said program transistor of each branch have a common floating gate and separate control gates;

said control gates of said program transistors are connectable to a program voltage;

a drain of each program transistor is connected to a respective input node;

said control gate of said read transistor in each branch is connected to the output node of the other branch;

the method comprising the steps of:

holding ~~the~~ input voltages that are applied to the input nodes of the program transistors at logic low level in a static mode; and

raising at least one of said ~~the~~input voltages to a voltage value high enough to generate hot electrons or hot holes at the drain ~~of a respective transistor~~of the program transistors in a program mode.

8. (Currently Amended) The method according to claim 7 further comprising:

connecting the program voltage ~~to the~~ of the control gates of the program transistors to a common supply voltage in the static mode; and

raising said program voltage to a voltage level high enough to attract electrons or holes into the floating gate in the program mode.

9. (Currently Amended) ~~The bi-stable latch circuit according to claim 2, wherein said drain and source line are~~ A bi-stable latch circuit having a pair of cross-coupled branches, each branch including a complementary driver and a load and connected between a drain line and a source line, and each branch providing a non-volatile memory cell having a program transistor and a read transistor, wherein at least one of the driver and load of each branch includes the corresponding read transistor; said driver and load of each branch are connected in series and provide a respective output node; said read transistor and said program transistor have a common floating gate and separate control gates; the control gate of said program transistor is connectable to a program voltage; a drain of each program transistor is connected to a respective input node; and said control gate of said read transistor in each branch is connected to the output node of the other branch;

wherein at least one of said read transistor and program transistor is a semiconductor device using hot electron injection for changing a threshold voltage thereof;

and wherein said drain and source line are connectable across a common supply voltage in a static mode ~~but~~and at least one of said drain and source ~~line~~lines is ~~disconnected~~disconnectable from said common supply voltage in a program mode.

10. (New) The bi-stable latch circuit according to claim 9, wherein each read transistor being a part of the driver in each branch.